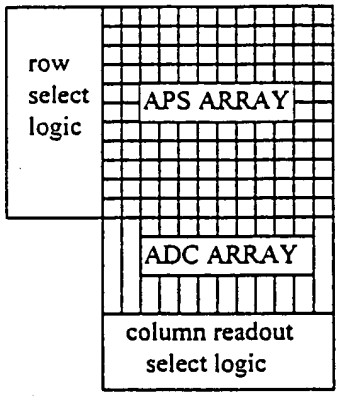
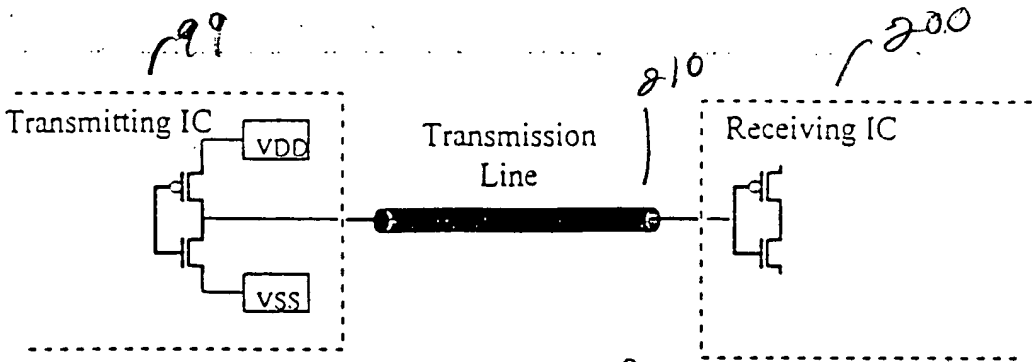



**Figure 1 column parallel architecture for focal plane A/D conversion**




99 210 200

(a) FIG 2

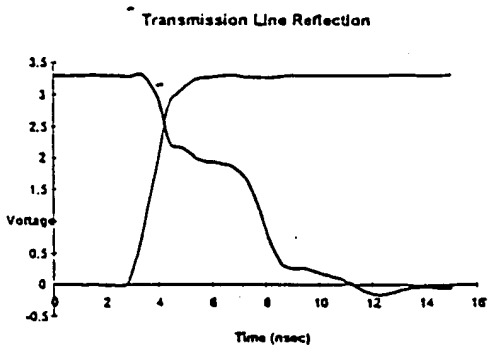
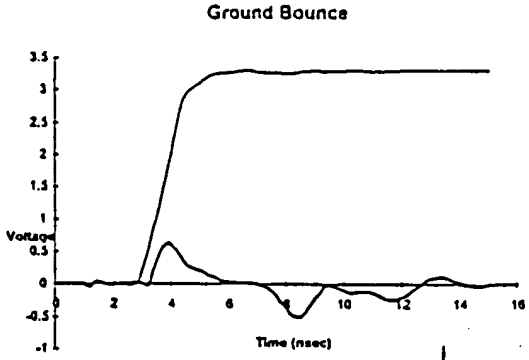



FIG (b) 3a




(c) Fig 3b

**Figure 1 (a) Conceptual diagram of standard CMOS I/O. (b) Output waveform when driving 1ft of coax cable. (c) Glitch voltage at the transmitter ground line.**

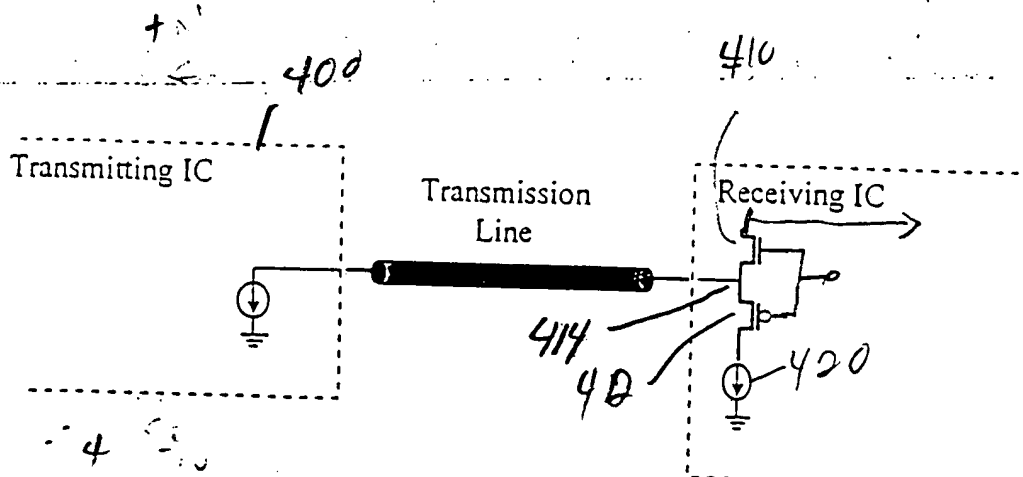



Figure 1 Conceptual sketch of CMOS current mode I/O technique

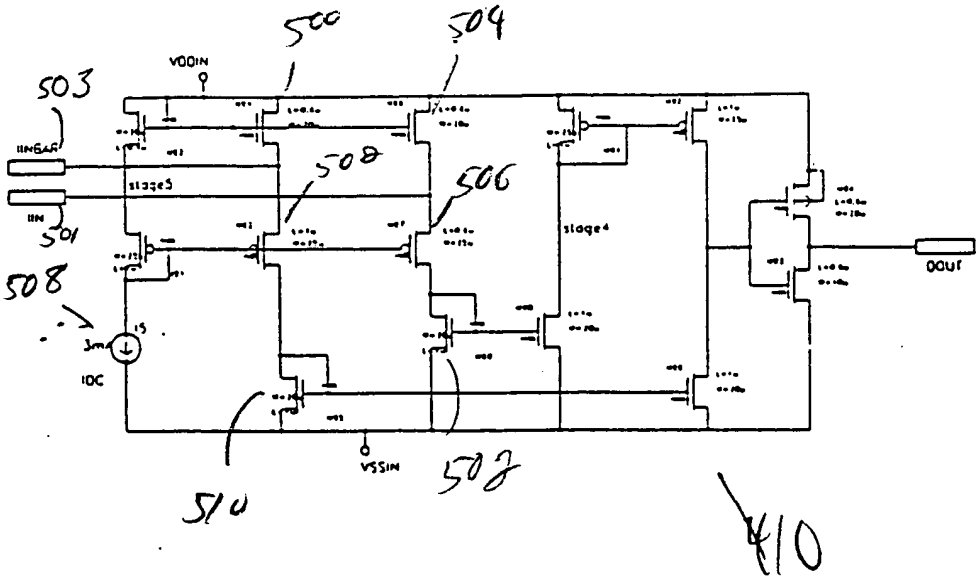



Figure 5 Schematic of receiver circuit.

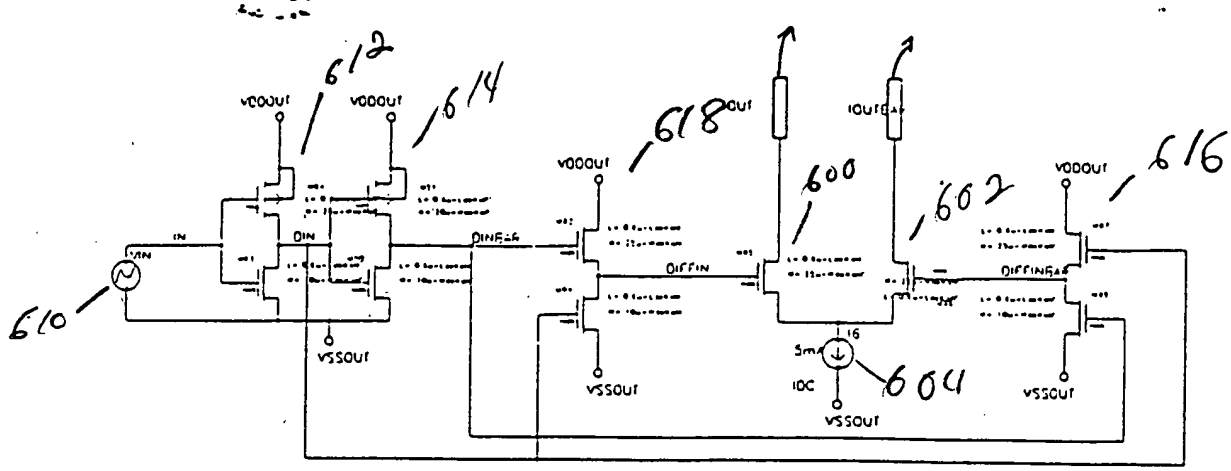



FIG 6

(a)

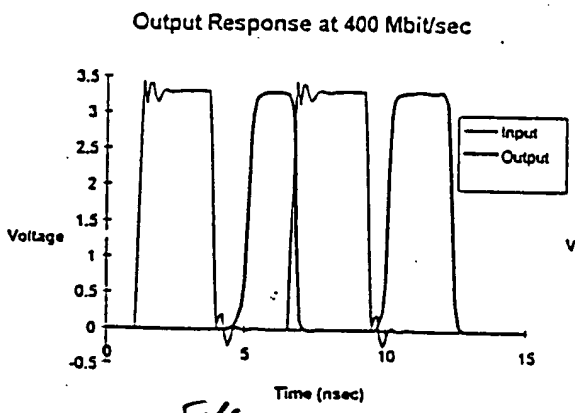



FIG 7a (b)

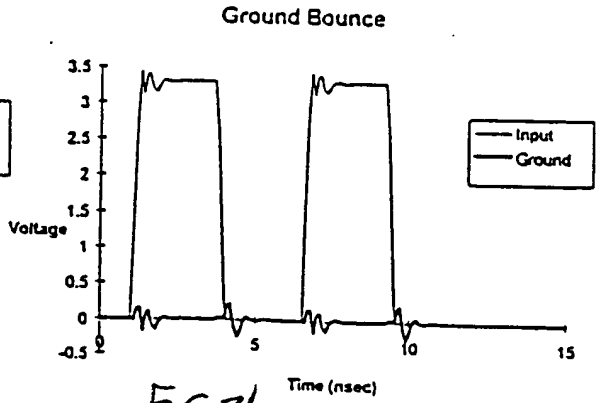



FIG 7b (c)

**Figure 6** (a) Schematic diagram of 1st output buffer. (b) Output waveform. (c) Glitch voltage at the ground line.

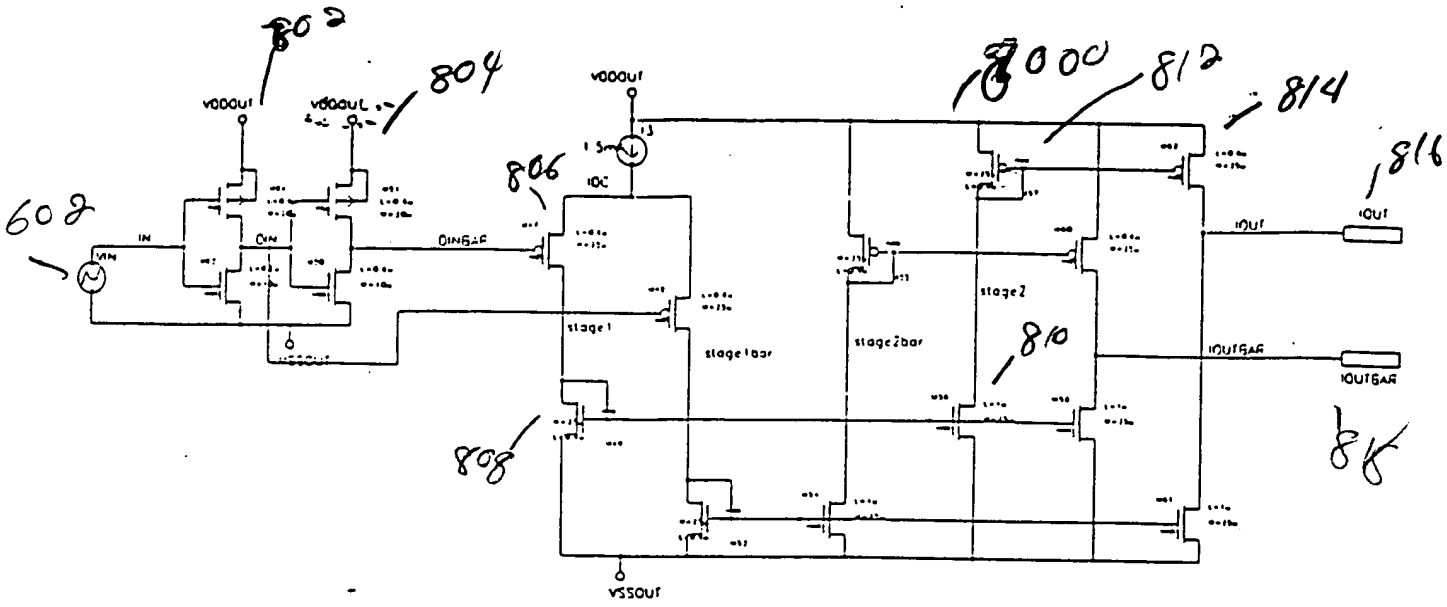



FIG 8

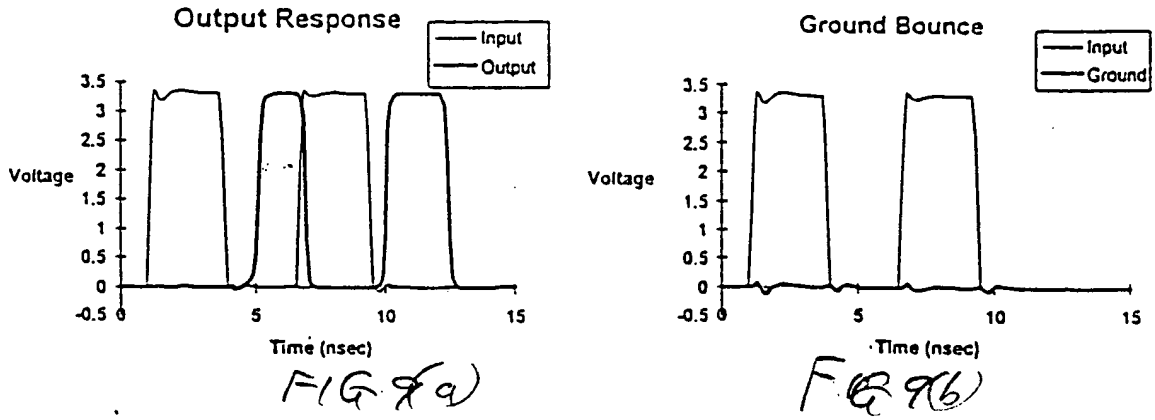



FIG 9(a)

FIG 9(b)

Figure 8(a) Schematic diagram of 2nd output buffer. (b) Output waveform. (c) Glitch voltage at the ground line.